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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,220	05/09/2001	Shunpei Yamazaki	SEL 259	4950

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EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,220	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see # 7, filed on 08/30/04 with respect to the rejection(s)of claim(s) 1-45 under U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shinotsuka et al. (USPN 6191408).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (USPN 6107983) in view Shinotsuka et al. (USPN 6191408).

Regarding claim 1, 7 and 13, Masuda teaches a liquid crystal display device (101) with a substrate (111), which includes driver circuits (210a, 201b, 301a, 301b), and a plurality of thin film transistors, TFTs (165) coupled with pixel electrodes (col. 5, lines 28-46 and Fig. 2). Masuda also teaches that the driving circuit (201a) includes a logic circuit section (215a), which in turn includes two 2-input NAND gates NA1 and NA2 (col. 6, lines 34-45 and Fig. 3). Furthermore, Masuda points out the use of a decoder having a plurality of logic circuits (col. 1,

lines 60-67 and col. 2, lines 1-5. However, Masuda does not teach all semiconductor elements being n-channel type semiconductor elements. Shinotsuka on the other hand discloses a semiconductor fabrication process in which type of transistors used are n-channel MOS transistors (Q1, Q2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's display system to adapt Shinotuska's semiconductor fabrication, which includes use of n-channel MOS transistors. One would have been motivated in view of the suggestion in Shinotsuka the use of n-channel MOS transistors equivalently yields the desired n-channel type semiconductor elements. The use of MOS helps form an image sensor 1 displayable is on the display unit 13 as taught by Shinotsuka.

Regarding claims 4, 10 and 14, Shinotsuka's Fig. 2.

Regarding claims 2, 8 and 15, see Masuda's Fig. 2 (111).

Regarding claims 3, 9 and 16, Masuda teaches the use of TFT (165). See Fig. 2.

Regarding claims 5-6, 11-12, and 17-18, Masuda teaches the use of the liquid crystal projector 1 with three liquid crystal display devices 101, 501 and 601.

Claims 19-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (USPN 6107983) in view of Shinotsuka et al. (USPN 6191408) and in further view of Lei (USPN 6169391).

Regarding claims 19 and 24, Masuda in view of Shinotsuka has been described. However, Masuda as modified does not teach first and second semiconductor elements such that a gate of the second semiconductor element is connected to a drain of the first semiconductor

element. Lei on the other hand illustrates the use of transistors (Fig. 7, and Fig. 9) where a gate of transistor (51) is connected to a drain of transistor (46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's display system to incorporate Lei's arrangement of transistors. One would have been motivated in view of the suggestion in Lei that the transistors (51, 46) as configured in Fig. 7 satisfy the desired arrangement of the two semiconductor elements. The use of transistors helps achieve a low voltage direct current for display indicators such as light emitting diodes as taught by Lei.

Regarding claims 28, 32, 36 and 41, Masuda in view of Shinotsuka. has been described. In addition, Masuda teaches either one of the scanning line drive circuits 201a, 201b and video signal line drive circuits 301a, 301b or, one of sets of drive circuits 201a, 201b and 301a, 301b is constructed of a plurality of stages of shift registers. Lei teaches N channel depletion mode transistor switch and N enhancement mode transistor switch. See fig. 7 and Fig. 9 respectively.

Regarding claims 20, 25, 29, 33, 37-38 and 42-43, Masuda teaches a pair of electrode substrates111 and 191.

Regarding claim 21, Masuda teaches the use of TFT (165). See Fig. 2

Regarding claims 22, 30 26, 34, 39 and 44, Masuda teaches the use of a plurality of display pixels arranged in a matrix array; also see Fig. 9

Regarding claims 23, 27, 31, 35, 40 and 45, Masuda teaches the use of the liquid crystal projector 1 with three liquid crystal display devices 101, 501 and 601.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts are cited for further reference.

U.S. pat. No. 6,084,461 to Colbeth et al.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

January 7, 2005

XIAO WU
PRIMARY EXAMINER